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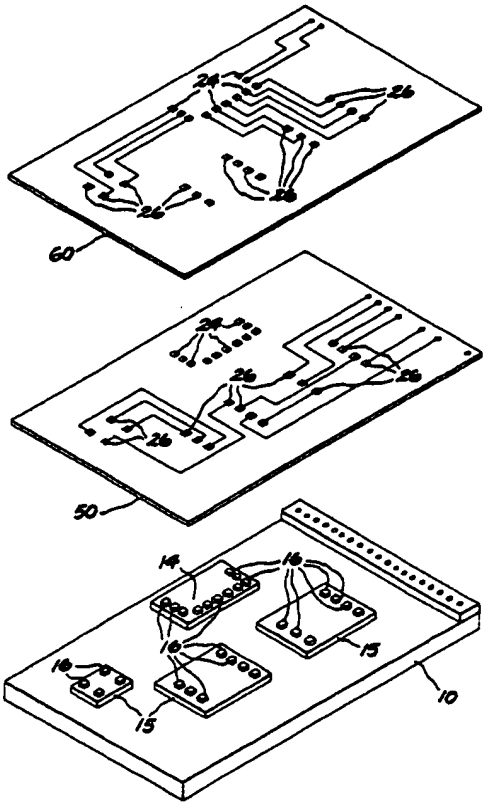
(57) Abstract

The utilization of a removable overlay layer (50) together with its associated metallization pattern, is used to effectively provide wafer scale integration for integrated circuit chips. The method and configuration of the present invention provide for the fabrication and testing of systems which are otherwise untestable. The present invention also permits integrated circuits systems (15) to be tested in their final configuration in terms of speed and operating environment and the invention eliminates many of the problems associated with wafer or chip probes. The present invention also utilizes special test chips (14) which are either temporarily or permanently affixed in an integrated circuit chip package.



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METHOD AND CONFIGURATION FOR TESTING ELECTRONIC CIRCUITS AND INTEGRATED CIRCUIT CHIPS USING A REMOVABLE OVERLAY LAYER

Background of the Invention

The present invention relates to packaging electronic integrated circuit chips into operable chip systems in a manner to facilitate testability. More particularly, the present invention relates to a method and configuration employing one or more removable overlay layers containing interconnection metallization patterns. Even more particularly, in one embodiment of the present invention, test chips are packaged with the system chips to exercise the system in its final configuration.

The present invention is generally directed to a method for interconnecting integrated circuit chips so as to allow them to be tested in their final configuration in terms of speed, operating environment packaging, temperature, voltage and proximity to other chips of the system. In the present invention, a removable overlay layer is applied to chips positioned on a substrate. The interconnection pattern of the overlay layer is specifically designed to partition the system for easy testing. The interconnect density of the overlay structure and its very low capacitive loading permit the utilization of extremely high density patterns which can make interconnection to a chip possible, otherwise, chip systems cannot easily be tested. Probe stations are inadequate for such purposes because too many probes would be required or because the chip pads are too small to accommodate a probe or because the capacitive loading of the probe station is too high to allow the chip to operate at maximum speed.

Special test chips may also be employed herein. These test chips are placed on the substrate along with the operating chip or chip system for the purpose of testing circuits at speeds and under operating conditions which cannot be duplicated at the wafer probe level.

The overlay layer employed herein is removable and there is no resulting degradation to the underlying chip. The overlay layer can be removed and reapplied several times if necessary with different wiring configurations and with removal and replacement of defective chips until the final operating configuration is established. Alternate overlay configurations are possible. In one configuration, inferior, but easily processed materials are used to provide a test overlay layer thereby simplifying the process and exposing the chips to less stringent processing conditions. In a second configuration, a test overlay layer is applied over an already in place overlay layer for the purpose of simplifying partitioning and multiprobe testing of a complex system.

The method and configuration of the present invention is unique in that chips can be arranged in their final operating positions, and connected for the purpose of testing. Then all connections are removed and are reconnected in an operating configuration. Other interconnect systems, including hybrid circuits, printed circuits and hard-wiring are not amenable to easy removal of all interconnects and reapplication of the interconnections in a different form.

The problem to be solved is a multi-faceted one. The generic problem is to test a system at the lowest feasible functional level to identify defective parts so that a completely functioning system with a high degree of assured reliability can be produced. A first set of

problems results from the deficiency of probing chips at the wafer level. Wafer probers are limited in speed of the chips that they can test due to the relatively long runs and high capacitive loading associated with the probes. Wafer probes are also limited in the total number of chip pads which can be probed at one time. Wafer probes are also limited to the maximum size of the pad which can be probed. This limitation is exacerbated by large numbers of pads. Additionally, increased pin count is also becoming more prevalent with the advent of very large scale integration since more complexity can now be put on a given chip.

Another problem exists in testing systems where several chips must be interconnected to perform a given function. In particular, it may be impossible to detect a defective part until it is interconnected with other parts of the functional block. Examples of such cases include multiple chip microprocessor systems, fast fourier transform systems in which the system size is too large for a single chip, large parallel multiplying systems, and memory systems. It is possible to test the functional blocks after they are assembled into a complete system. However, testing would now be extremely complex and time consuming due to the constraints imposed by the large number of parameters which must be tested.

An additional problem is testing chips under burn-in conditions. The typical burn-in involves operating the system typically for a period of approximately 100 hours at high temperature conditions. Experience has shown that if a chip is apt to fail, it generally fails under these conditions within the 100 hour time period. The conventional approach to testing chips is to first test the chip at the probe station, recognizing deficiencies in the number of probes and in speed. The chips which pass these tests are

packaged. In high reliability systems, the packaged chips are burned-in under power. After burn-in, the package chips are tested again to determine proper functionality. The packaged chips are then interconnected on a printed circuit board to form the final system. Because of size and speed constraints, it is desirable to incorporate several chips in the same package. This complicates burn-in because one failed chip in a package requires that the whole package, including all the good chips, be discarded. The high density interconnect system disclosed herein uses an overlay layer to provide a method for directly connecting a large number of chips within the same package. The invention disclosed herein provides a method for the complete test and burn-in of the chip as well as a practical method for partitioning the system into manageable blocks which are easily tested. In addition, in an alternate configuration in which the test layer is added after the overlay layers have been interconnected, a removable overlay layer can be used to provide a multiplicity of connections throughout the rest of the system for the purpose of system testing and debugging during and after burn-in. This approach provides the rough equivalence of a "bed of nails" test fixture which is typically used for printed circuit boards but on a pitch of 1 mil rather than a pitch of 50 mils.

Summary of the Invention

In a preferred embodiment of the present invention, an integrated circuit chip package comprises a substrate together with a plurality of integrated circuit chips affixed to the substrate. The integrated circuit chips have interconnect pads thereon for connections to other chips or to different parts of the same chip. A polymer film overlay is disposed over the chips and the

substrate. The film possesses apertures aligned with at least some of the interconnect pads. The polymer film also contains a metallization pattern disposed on the film and operating to connect select interconnect pads. Most importantly, for the present invention, the package also includes at least one test chip disposed on the substrate and being operable to test at least one other of the chips on the substrate.

In accordance with another embodiment of the present invention, a method for producing integrated circuit chip packages begins by affixing a plurality of integrated circuit chips to a substrate. The integrated circuit chips possess interconnect pads, as described above. At least one test integrated circuit chip is also disposed on the substrate. The test chip includes means thereon for testably driving at least one of the other chips on the substrate. Then, a polymer film is disposed over the test chip and the other chip or chips. As above, the polymer film possesses a plurality of apertures, at least some of which are aligned with the interconnect pads, together with a layer of metallization for connecting selected pads on the test chip to selected pads on the other integrated circuit chips. It is noted that more than one test chip may be employed and that these test chips may include memory functions.

In yet another embodiment of the present invention, a method for producing integrated circuit chip packages includes a step of affixing a plurality of integrated circuit chips to a substrate. As above, the chips possess interconnect pads. Then an overlay layer is applied to the chips and to the substrates. The overlay layer includes a metallization pattern for connecting the chips in a first configuration. This configuration is then preferably tested after which the first overlay layer is removed

and a second overlay layer is applied so as to connect the chips in a second configuration. In general, the second configuration is the one in which all parts of the system are connected for final use. It is noted that in this embodiment, the utilization of a test chip is not required.

Accordingly, it is an object of the present invention to provide a method for testing unpackaged interconnected circuits so as to cause minimum capacitive loading on the chips under test so as to thereby allow tests to be conducted at maximum speed.

It is also an object of the present invention to provide a method for testing which allows chips to operate in their final locations such that temperature and environmental conditions (such as electromagnetic interference, radio frequency interference and power supply variations) are all substantially identical to the final desired configuration.

It is yet another object of the present invention to provide a method for testing which allows long term burn-in of chips without tying up expensive test equipment.

It is a still further object of the present invention to provide a method for testing which allows the utilization of special chips, thereby eliminating the need for expensive high speed test equipment, allowing the combination of a multiplicity of chips to be tested at once and reducing the number of external connections or package pins required.

Another object of the present invention is to provide a method in which chips can be tested completely with a pad count which exceeds the capability of probe testing with pad sizes which are below the capacity of probe testing.

Yet another object of the present invention is to provide for functional testing of multiply interconnected chips.

It is a still further object of the present invention to provide multiple testing configurations by completely changing the interconnect wiring for one or more chips in the system.

Yet another object of the present invention is to provide a method of making a removable interconnection to a multiplicity of points in an integrated circuit chip system already connected by an overlay interconnect method, thereby allowing for complete system test with minimal increase in external probe, pins and drivers.

Lastly, but not limited hereto, it is an object of the present invention to effectively provide wafer scale integration packages without the concomitant reliability and yield problems associated therewith.

Description of the Drawings

The subject matter which is regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of practice, together with further objects and advantages thereof, may best be understood by reference to the following description taken in connection with the accompanying drawings in which:

Figure 1 is an exploded isometric view illustrating a multichip circuit with a test overlay layer;

Figure 2 is an exploded view similar to Figure 1 but more particularly showing the utilization of a special test chip connected to the other chips in the circuit by means of a different overlay layer;

Figure 3 is an exploded isometric view illustrating a multichip circuit package with operational overlay layer;

Figure 4A illustrates means to probe internal test points with a reduced number of external pins;

Figure 4B is a schematic diagram illustrating the use of memory means to supply test vectors and to store test results on a packaged substrate assembly;

Figure 4C is a schematic diagram similar to Figure 4B more particularly illustrating the utilization of a microcomputer chip to compute test vectors and to evaluate test results;

Figure 5 is an exploded isometric view illustrating a multichip circuit assembly which simultaneously employs an operational circuit overlay layer and a test overlay layer.

Detailed Description of the Invention

A related patent application Serial No. (RD-17,433) describes a method and apparatus for applying a removable polymer overlay layer. A second related patent application Serial No. (RD-17,428) describes a preferable method for supplying the overlay layer with a pattern of apertures for connection to the above-described interconnect pads. A third related patent application Serial No. (RD-17,432) describes a method for providing a preferred form of metallization patterning over a polymer film. All three of these applications are hereby incorporated herein by reference. These applications are assigned to the same assignee as the present invention.

The first of the aforementioned patent applications in particular discloses a method involving few steps and using easy-to-use materials. The methods disclosed

therein are generally more suitable for test layers since the test layer is easily processed and easily removed and since long term thermal and hydrolitic stability is not required.

Figure 1 shows an exploded view of a multichip circuit with overlay layer 20 configured so as to test chips 15 on substrate 10. In a preferred embodiment of the present invention, chips 15 are affixed to substrate 10, as by bonding in place by conventional means using epoxy bonding, thermoplastic bonding, or eutectic die bonding. Polymer overlay layer 20 is applied by the following method. Two coats of a solution of methylmethacrylate in THF (tetrahydrofuran) are sprayed over chips 15 with interconnect pads 16. Each coat is dried at a temperature of approximately 150°C for a period of about 5 minutes. A sheet of acetate film 1 mil in thickness is laminated to the top of the chips and to package pins 11. A vacuum pressure laminator is preferably employed. Details of a vacuum pressure laminator can be found in application Serial No. (RD-17,433) above. Preferable lamination conditions comprise a pressure of approximately 30 pounds per square inch at a temperature of about 120°C for a period of about 3 minutes. The substrate is then cooled to 80°C and removed from the laminator. Via holes over the appropriate chip pads and package pinout pads are fabricated using a focused laser according to the method outlined in patent application Serial No. (RD-17,428). Plasma etching is accomplished using somewhat less stringent conditions than required for high stability polymers. For example, one may employ an atmosphere of 30% CF_4 and 70% oxygen at a pressure of about 0.4 torr and at a power level of 200 watts for 6 minutes using a Branson IPC 2000 barrel etcher. Metallization is preferably provided by sputtering a 1,000 angstrom thick layer of titanium, followed by a

layer of 1 micron thick copper. The metallization is preferably patterned by spraying or spinning a coating of photoresist on the copper surface, drying for about one half hour at approximately 90°C and exposing the positive resist material with a scanned ultraviolet laser under control of computerized artwork. A preferable photoresist material includes Dynachem OFPR 800 photoresist. Details of a preferred laser exposure system are disclosed in patent application Serial No. (RD-17,428). After development of the photoresist, the desired metallization pattern is etched using an acid mix comprising 600 grams of nitric acid, 600 grams of sulfuric acid and 600 grams of H_3PO_4 in 1.5 liters of water to remove the copper layer, if present. A mixture comprising 1 part fluoroboric acid and 9 parts water is used to remove the titanium layer. The circuit is now ready for testing according to the metallization pattern illustrated in Figure 1. The pattern of Figure 1 is used to connect package pins 11 to pads 16 on each chip 15, as required for testing. All testing is conducted by applying signals to inputs through the package pins and observing the resultant outputs at the package pins, at least in the embodiment illustrated in Figure 1. It is noted that via holes 26 are aligned with pads 16 on chips 15. It is also noted that vias 21 are aligned with package pins 11. It is further noted that metallization patterns 22 generally extend from via openings 21 to via openings 26 at least for the sample test configuration shown. This pattern may, however, vary over a wide range of patterns.

Figure 2 illustrates an alternate embodiment of the present invention in which test chip 14 is used. Test chip 14 is connected to metallization patterns on overlay layer 20' by means of via openings 24. It is seen in Figure 2 that overlay layer 20' now makes connections between chip

pads 16 and test chip 14. It is noted that more than one test chip may be employed even though the figure illustrates only a single one being used. In the example illustrated in Figure 2, only two connections 23 are shown as being required between the test chip and the package pins. It can be seen through the use of the test chip that packaging pins can be conserved.

The configurations of Figures 1 or 2 may then be employed to test chips 15. Following the testing, overlay layers 20 or 20' may be removed. Defective chips may be removed or reconfigured or repositioned on the basis of test results obtained. Subsequently, an operational circuit overlay layer 20'' may be applied to the chip configuration. As a result, the system illustrated in Figure 3 may be produced. It is noted that the chief difference between Figure 1 and Figure 3 is the particular metallization pattern employed.

Figures 4A, 4B and 4C show three alternate implementations of test chips. In all cases, these configurations consist of circuits and technologies well known to those skilled in the art.

Figure 4A illustrates an array of three transmission gates 38 (typically in CMOS technology). One of the three transmission gates can be selected by selection logic 37. Under control of the test apparatus, the iata selector applies the appropriate signal voltages to transmission gates 38 to turn one of the three gates on and to connect external pad 34 to one of three or more possible internal connection points. It is clear that a number of internal connection points can be multiplexed to one outside pin by this method. The very high density interconnect capability afforded by the overlay layer allows this method to act as a multiprobe connection system.

Figure 4B illustrates an alternate embodiment of the present invention in which memory means 32, such as a random access memory, is employed as a vector generator to supply test vectors to the inputs of a chip or group of chips 15 under test. The output of the chip or group of chips is stored in second memory means 33 also typically comprising a random access memory. Counter 31 driven by clock 30 provides sequential addresses to sequence the output of test vectors and the storage of test results. This system can be run at very high speed, limited only by the speed of the memory means selected. The test vectors are supplied at a much more leisurely pace through external input pins 35. Inspection of the results is achieved in a much more leisurely pace by supplying the contents of memory means 33 to external pins 34. This shows an example of very high speed testing taking place through interconnections in the overlay layer with lower speed connections controlling the testing through external pins 35. It is noted that lines having a hash mark (/) denote multiple signal and/or control paths.

Figure 4C shows a completely internal configuration for high speed testing. In this configuration, microprocessor 40 computes test vectors and supplies them to vector generation random access memory 32. When the requisite number of vectors are input to the memory, the memory is sequentially accessed by the associated counter and the output memory supplies the inputs to a chip or a group of chips 15 under test. The resultant outputs from the test are stored in second memory means 33. At the end of the cycle, microprocessor 40 reads the test results and compares them to computed results to determine if errors have occurred. In this configuration, the entire system can be tested over a long period of time under temperature and

variations of environmental conditions such as electromagnetic interference without any connection, other than power supply, to the outside world. Microprocessors can be used to store test results inconsistent with the expected results, thereby identifying the specific chip or chip group and the failure which occurred, even when the failure occurs on an intermittent basis. Microprocessor 40 is accessed via external pins 41.

When a given test is completed, the test layer is removed according to the following method. First, copper metallization is dissolved in a solution preferably comprising 600 grams of nitric acid, 600 grams sulfuric acid and 600 grams of H_3PO_4 in 1.5 liters of water for a period of about 1 minute. This removes copper, but does not attack either aluminum metallization typically present on the chip pads or titanium which is also preferably (though optionally) present as a barrier layer. Titanium is preferably removed by placement in a solution of fluoroboric acid for a period of about 15 seconds. The overlay polymer and adhesive can be removed in a solution of THF for a period of 2 minutes followed by immersion in another clean solution of THF for 1 minute. If a new test layer is to be applied, the test layer process as described above can be started immediately after a defective chip has been removed and a new one put in place. If the final operational overlay layer is to be implemented, a plasma etch to remove a residual polymer is also preferred. Etch conditions preferably include an atmosphere comprising 50% oxygen and 50% CF_4 at a total pressure of 0.4 torr for a period of about 2½ minutes in an IPC 2000 barrel etcher at a power level of approximately 300 watts. The final layer is then provided according to the process described in patent application Serial No. (RD-17,433). Figure 3 illustrates an exploded view of

tested chips on a substrate with an interconnection pattern for an operational circuit. Note that this pattern is completely different from the test patterns shown in Figures 1 or 2. Note also that the materials used for the final operational configuration preferably involve materials of long term thermal and hydrolitic stability such as KAPTON™ (supplied by Dupont de Nemours Company, Inc.) polyimide film. In addition, in the final operational configuration, the metallization used preferably comprises slightly thicker material to obviate any problems associated with electromigration or losses due to resistive paths.

An alternate approach involving the use of an overlay test layer is shown in an exploded view in Figure 5. This is the same circuit as shown in Figure 3 except that additional overlay layer 60 has been added to provide connections to the test chip or chips, and to the test pins of the package. Also note that operational circuit overlay layer 50 is similar to overlay layer 20'' illustrated in Figure 3 except for the presence of apertures 24 for connection to test chip 14. Test layer 60 can be added by spraying a solution of methylmethacrylate in THF and drying at a temperature of approximately 150°C for a period of 5 minutes. Two such coats are generally required. At this point, via holes are fabricated to the connection points on the layer below by using focused laser energy as described in above-mentioned application Serial No. (RD-17,428). Etch time in an oxygen plasma to clean out the apertures is relatively short since the layer is thin and since the material is highly susceptible to etching. Etch conditions of 200 watts for 4 minutes in an atmosphere comprising 30% CF_4 and 70% oxygen at a pressure of 0.4 Torr is sufficient. Metallization is preferably added by sputtering a layer of chrome which is approximately 1,000 angstroms thick,

followed by sputtering of sufficient copper for conductivity, typically 1 micron in thickness. Metallization is patterned, as described above, by a photolithographic method using an etchant of nitric acid, sulfuric acid and H_3PO_4 in water, as above. This etchant etches the copper but not the chrome. Chrome is etched in a cerric sulfate solution operated at 60°C. When testing is complete and the test layer is removed, it is easily removed by dissolving the copper in a copper etch solution. This etch attacks the copper, but does not attack the chrome layer. In this way, the underlying chrome layer protects the copper conductor of the underlying layer where it would be exposed at the interconnect points. The chrome is removed with a 25 second etch in the cerric sulfate sulfate solution. The test layer polymer dielectric can be removed in a solution of THF, followed by a second immersion in clean THF to remove any residue. The underlying KAPTON™ film of the operational interconnect overlay is totally uneffected by the THF solvent.

From the above, it should be appreciated that the method and configuration of the present invention fulfills all of the stated objectives. In particular, it is seen that a method is provided for testing integrated circuit chip subsystems to effectively provide wafer scale integration without its concomitant problems. Furthermore, it is seen that multi-chip integrated circuit systems can be constructed which would otherwise be untestable. It is also seen that the systems of the present invention can be tested in configurations substantially identical to their operating conditions in terms of capacitive loading, thermal environments and speed. It is also seen that the packaging method of the present invention permits the utilization of special test chips and thereby significantly reduces investment in

special test systems. It is also seen that special testing can be done off line and that testing is accomplished at very high speeds. Accordingly, it is seen that the method and configuration of the present invention significantly advances in the art of integrated circuit packaging.

While the invention has been described in detail herein in accord with certain preferred embodiments thereof, many modifications and changes therein may be effected by those skilled in the art. Accordingly, it is intended by the appended claims to cover all such modifications and changes as fall within the true spirit and scope of the invention.

THE INVENTION CLAIMED IS:

1. An integrated circuit chip package, comprising:

a substrate;

a plurality of integrated circuit chips disposed on said substrate, said integrated circuit chips having interconnect pads thereon;

a polymer film overlay disposed over said chips and said substrate, said film having apertures therein exposing at least some of interconnect pads; and

a pattern of metallization disposed on said film and connecting select interconnect pads through said apertures;

wherein at least one of said chips comprises a test chip operable to test at least one other of said chips.

2. The package of claim 1 in which said film is removable.

3. The package of claim 1 in which at least one of said chips is removable.

4. The package of claim 1 in which said substrate has external pins for circuit interconnection.

5. The package of claim 1 in which said at least one test chip is a microprocessor.

6. The package of claim 1 in which at least one chip includes memory means for storing test vectors.

7. The package of claim 6 in which at least one chip includes memory means for storing test result data.

8. The package of claim 7 in which said chips also include means for externally accessing said vector and said result memory means.

9. The package of claim 1 in which a second polymer film is disposed over said first film and said

metallization pattern together with a second metallization pattern disposed over said second film and connecting select interconnect pads.

10. A method for producing integrated circuit chip packages, said method comprising the steps of:

disposing a plurality of integrated circuit chips on a substrate, said chips having interconnect pads thereon;

disposing at least one test integrated circuit chip to said substrate, said test chip including means for driving said other chips; and

disposing a polymer film over said test chip and at least one other of said plurality of chips, said film having at least some apertures therein in alignment with said interconnect pads and said film having metallization patterns thereon for connecting select pads on said test chip to select pads on at least one other of said plurality of chips.

11. The method of claim 10 in which said substrate material is selected from the group consisting of glass, metal, ceramic, plastic, silicon and composites.

12. The method of claim 10 in which said polymer film is selected from the group consisting of thermoplastic materials and thermoset materials.

13. The method of claim 10 further including the step of operating said test chip so as to drive an interconnected configuration of said chips other than said test chip.

14. The method of claim 10 in which said test chip is a microprocessor.

15. The method of claim 10 in which said test chip includes memory means for storing a set of test vectors.

16. The method of claim 15 in which said test chip includes memory means for storing test result data.

17. The method of claim 13 further including the step of removing said polymer film and reapplying a second polymer film having apertures and metallization patterns thereon for connecting said chips in a second configuration.

18. The method of claim 17 in which said apertures and metallization patterns are determined in response to results obtained from said operating test chip.

19. A method for producing integrated circuit chip packages, said method comprising the steps of:

disposing a plurality of integrated circuit chips on a substrate, said chips having interconnect pads thereon;

disposing at least one test integrated circuit chip on said substrate, said test chip including means for driving at least one of said plurality of chips;

disposing a polymer film over said test chip and said plurality of chips, said film having at least some apertures therein in alignment with said interconnect pads and said film having metallization patterns thereon for interconnecting select pads on said plurality of chips;

disposing a second polymer layer over said first polymer layer and said first metallization patterns, said second layer having at least some apertures therein in alignment with said interconnect pads and said second layer having metallization patterns thereon for connecting select pads on said plurality of chips, one of said metallization patterns functioning to provide connections to said test chip for test functions and the other of said metallization patterns functioning to provide connections for achieving operational functionality.

20. A method for producing integrated circuit chip packages, said method comprising the steps of:

disposing a plurality of integrated circuit chips on a substrate, said chips having interconnect pads thereon;

disposing an overlay layer over said chips, said layer having at least some apertures therein in alignment with at least some of said interconnect pads, said layer also having a metallization pattern thereon for connecting said chips in a first configuration;

removing said overlay layer and said metallization;

applying a second overlay layer over said chips and said substrate, said overlay layer having at least some apertures therein in alignment with at least some of said interconnect pads, said second overlay layer also having a metallization pattern thereon for connecting said chips in a second configuration.

21. The method of claim 20 further including the step of testing said integrated circuit chips while connected in said first configuration.

FIG. 1

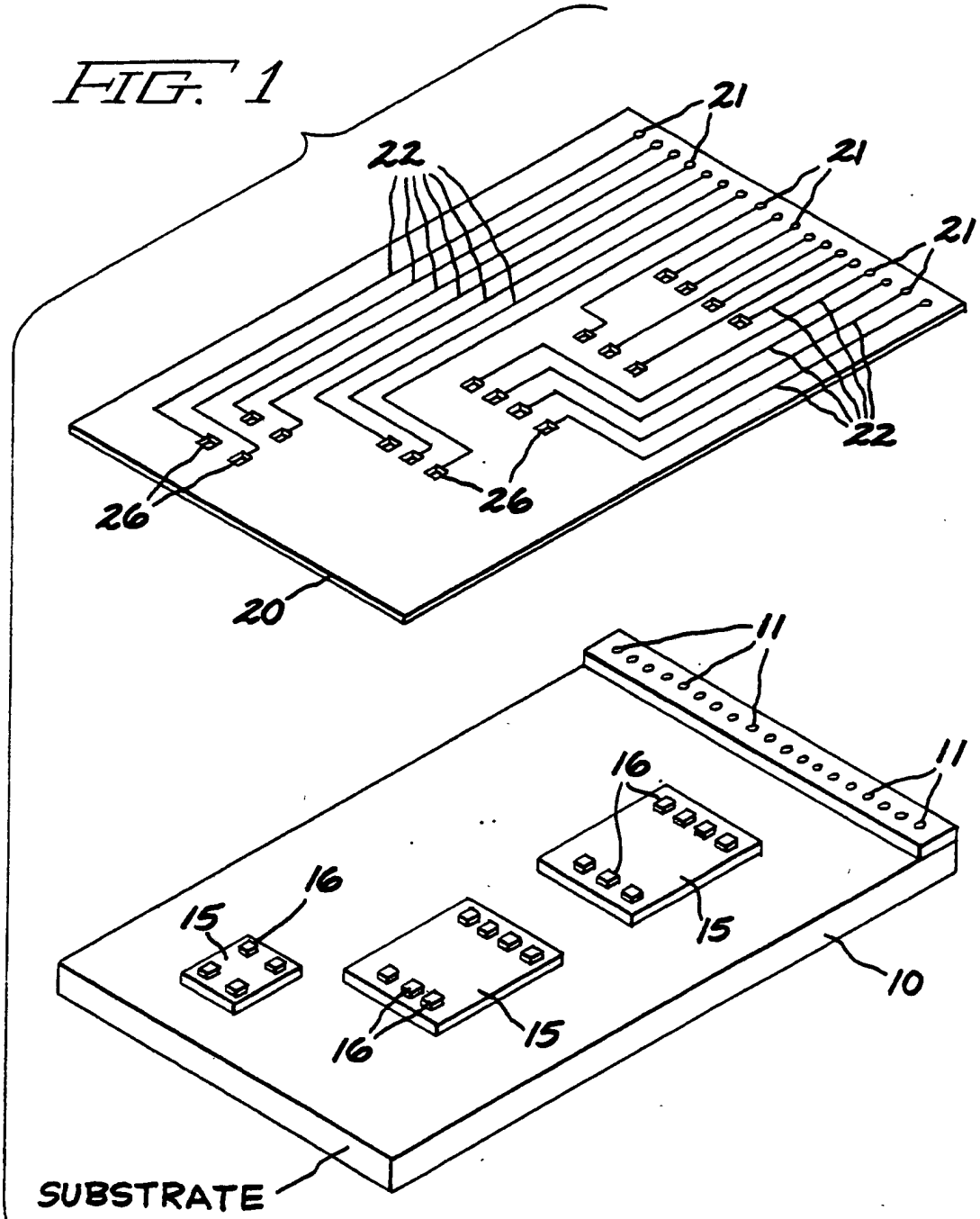


FIG. 2

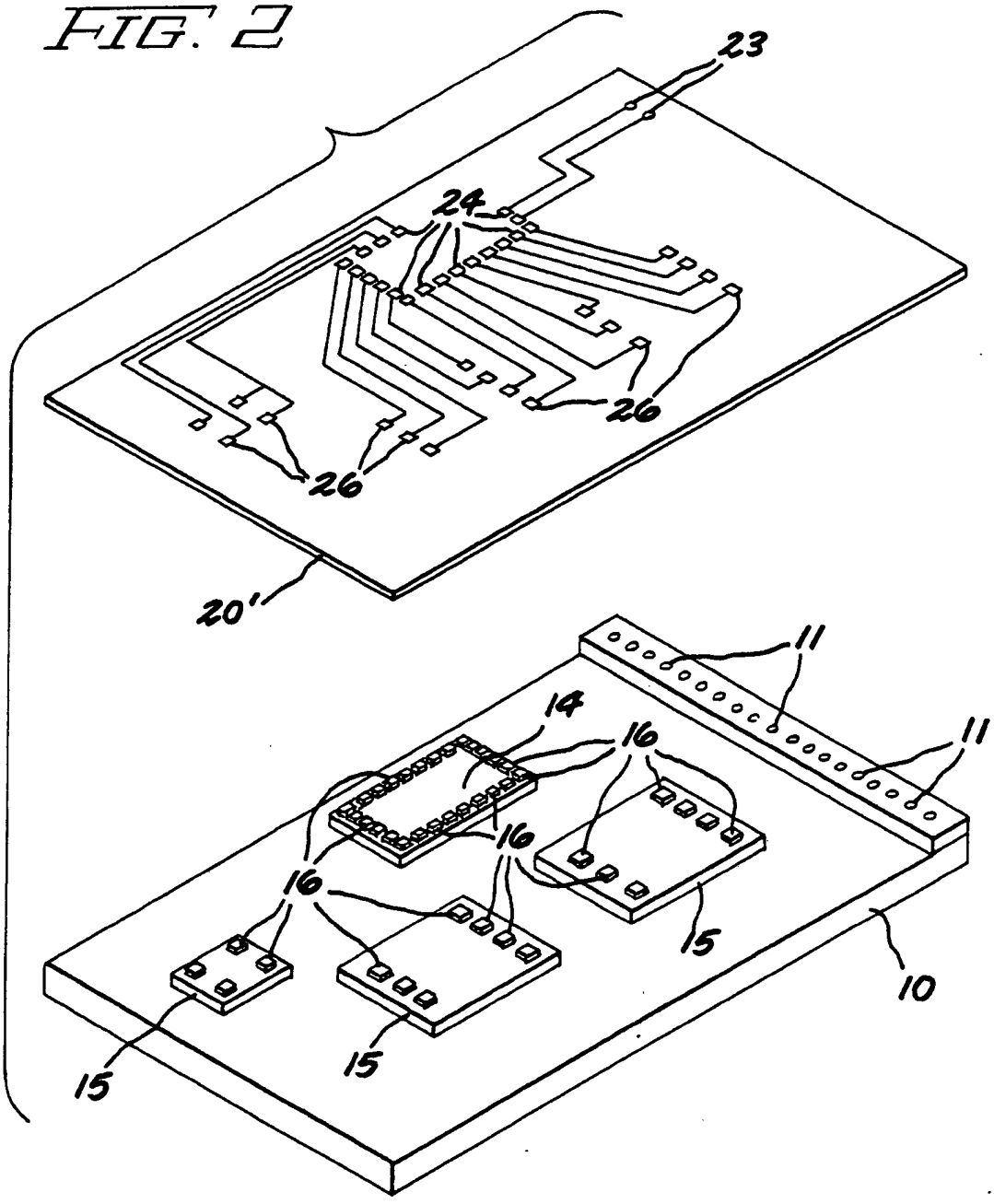


FIG. 3

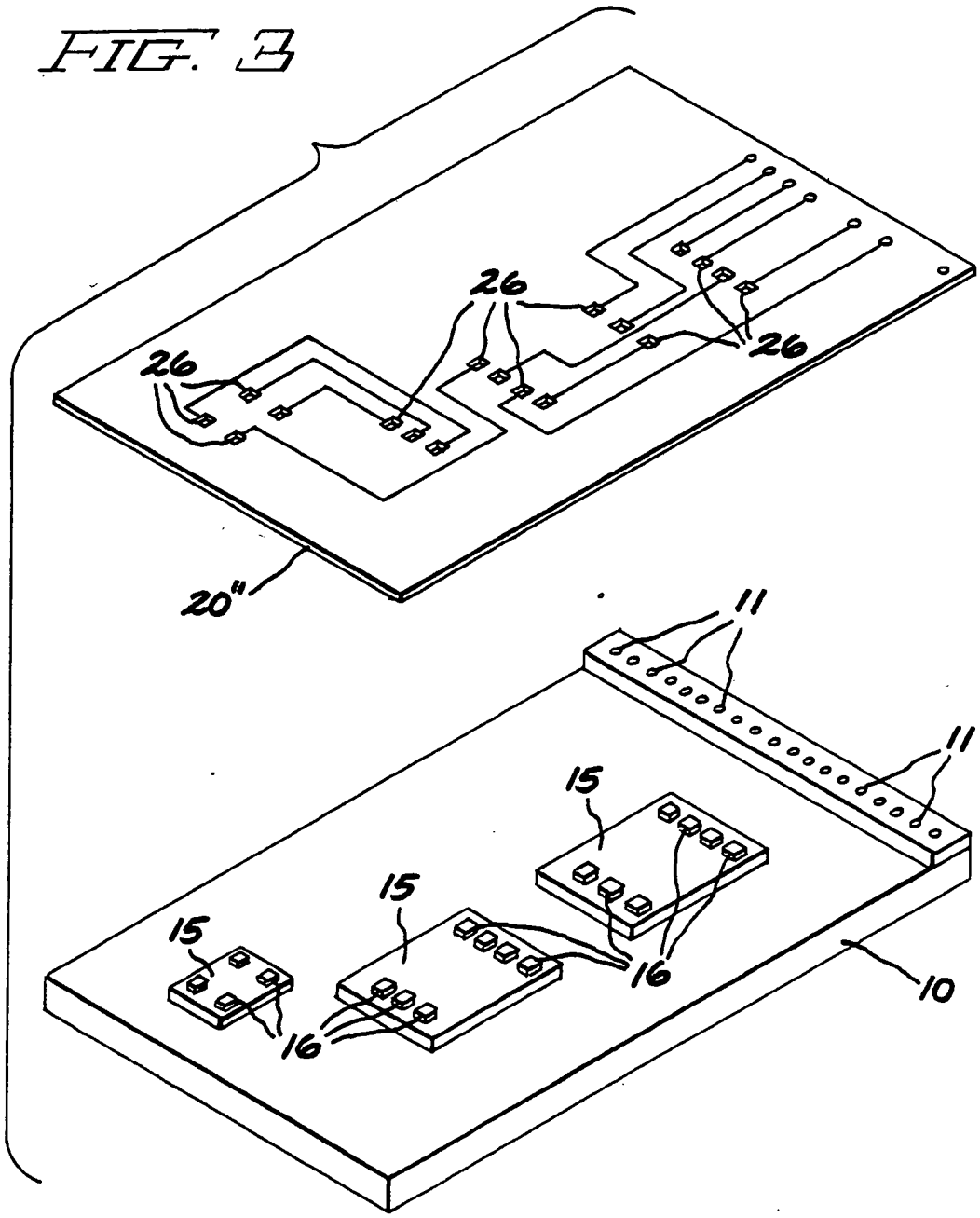
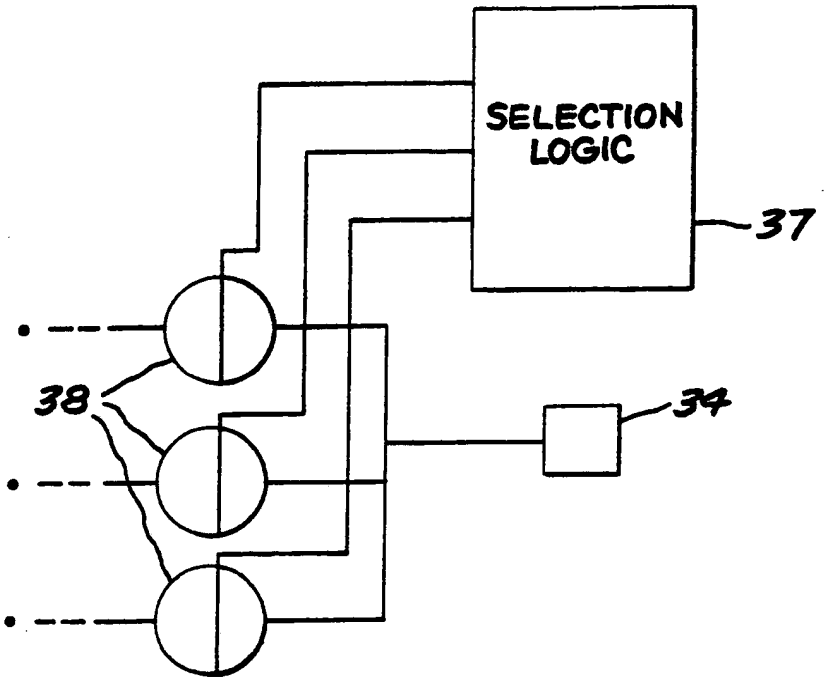
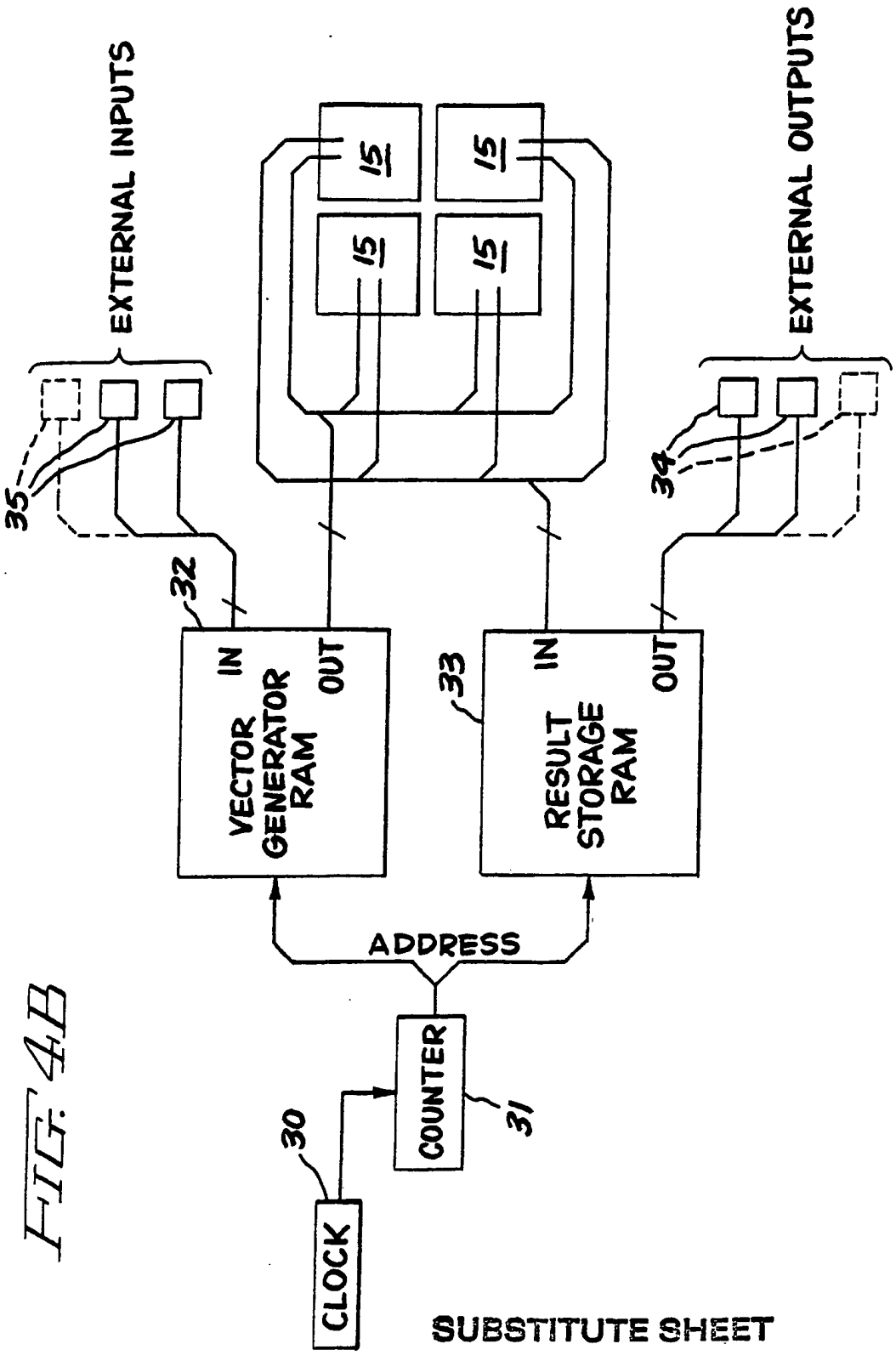


FIG. 4A




EXTERNAL INPUTS
EXTERNAL OUTPUTS
15
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34
32
33
IN
OUT
VECTOR GENERATOR RAM
IN
OUT
RESULT STORAGE RAM
ADDRESS
COUNTER
31
30
CLOCK

FIG. 4B

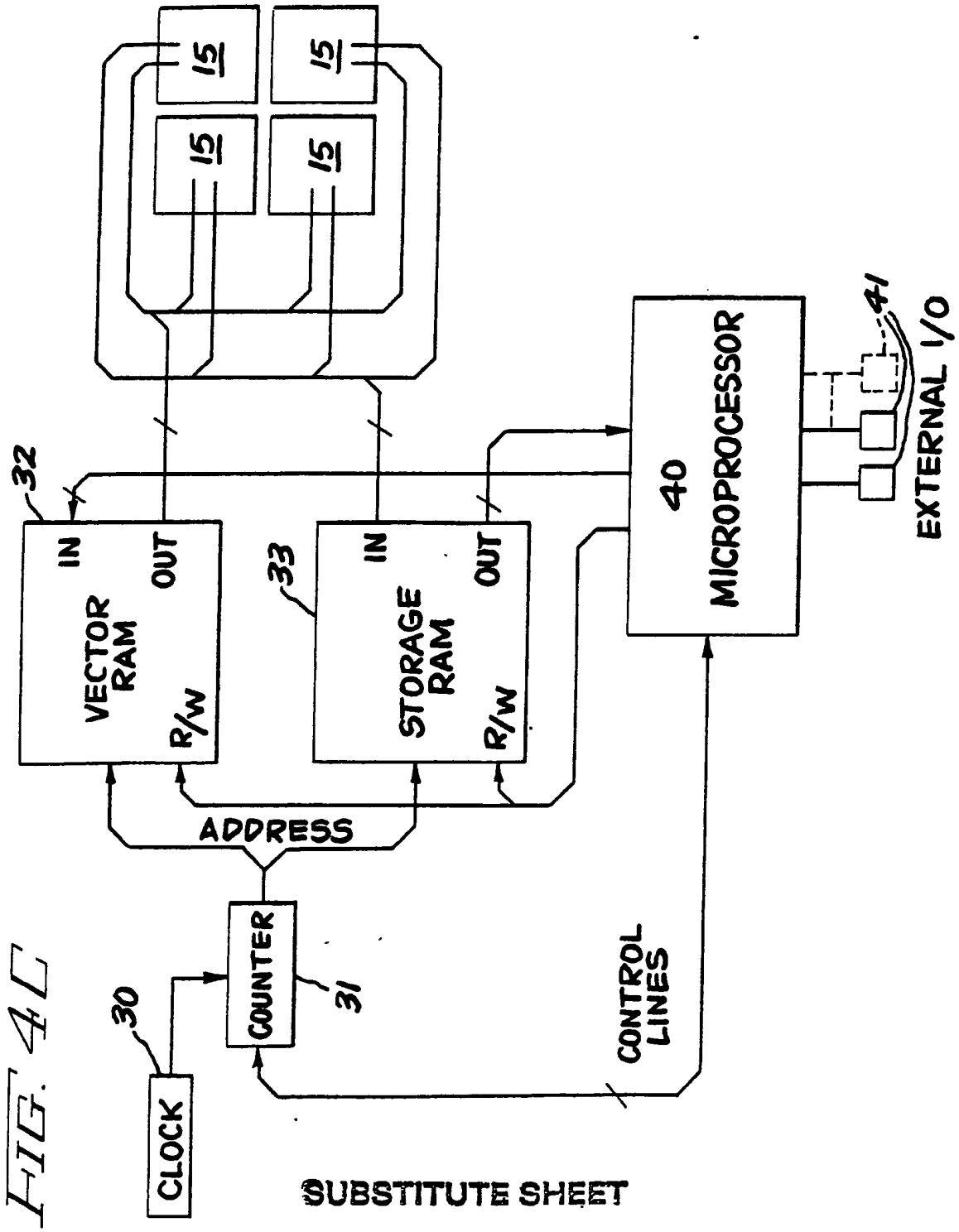
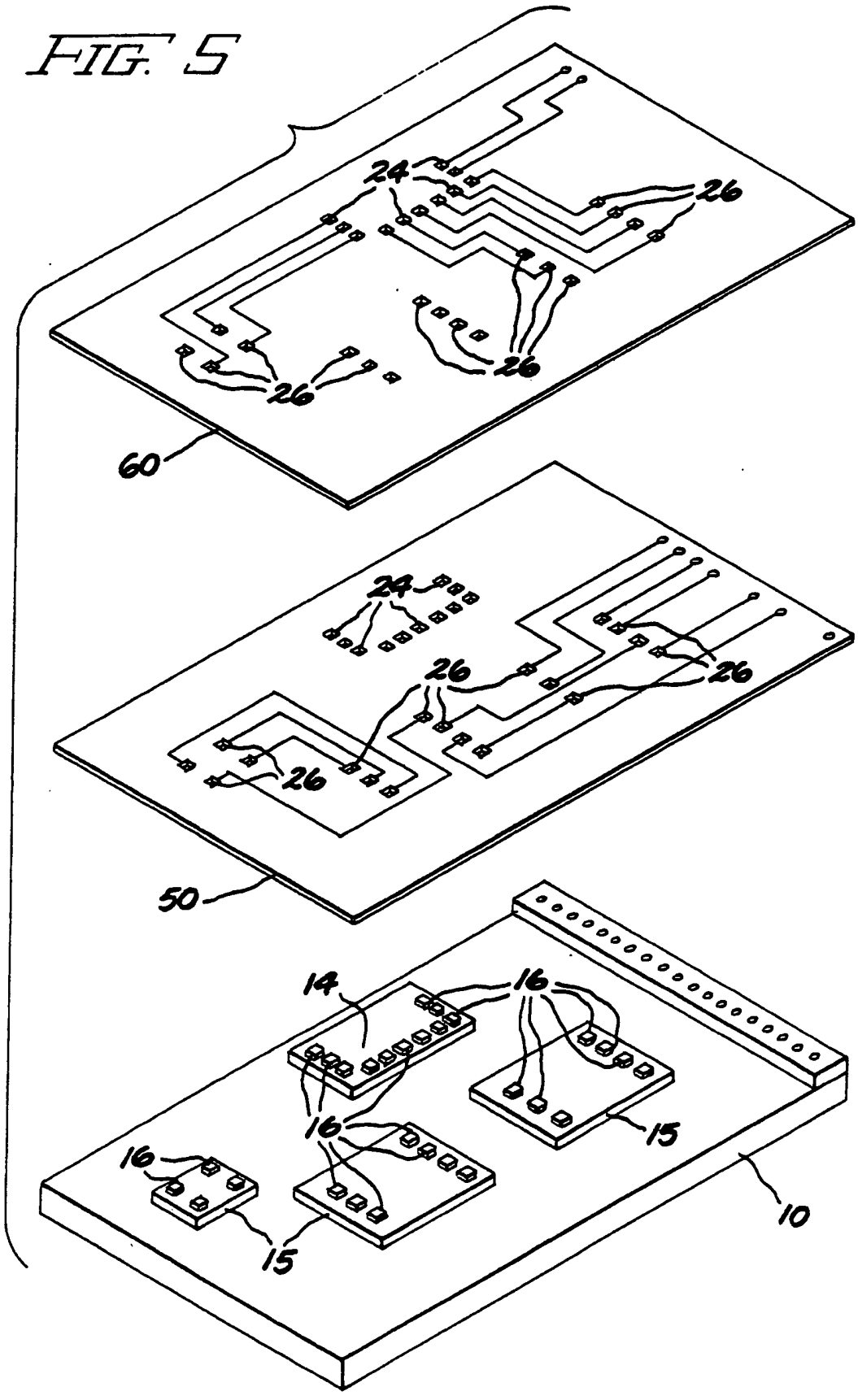

15
15
15
15
32
IN
OUT
VECTOR RAM
R/W
33
IN
OUT
STORAGE RAM
R/W
40
MICROPROCESSOR
41
EXTERNAL I/O
ADDRESS
COUNTER
31
30
CLOCK
CONTROL LINES

FIG. 4C

FIG. 5



INTERNATIONAL SEARCH REPORT

International Application No PCT/US 87/02473

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 01 K 21/66; H 01 L 23/52

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	EP, A, 0178227 (FUJITSU) 16 April 1986, see figure 3b; claims 1,12; page 8, lines 4-8	1
A	--	3,11
Y	Solid State Technology, volume 29, no. 3, March 1986, (Port Washington, New York, US), W. Lukaszek et al.: "CMOS test chip design for process problem debugging and yield prediction experiments", pages 87-93, see page 87, left-hand column, paragraph 1	1
A	-- EP, A, 0175870 (MOSAIC) 2 April 1986	
A	-- US, A, 4426773 (GENERAL ELECTRIC) 24 January 1984	
A	-- IBM Technical Disclosure Bulletin, volume 24, no. 2, July 1981 (New York, US), L.V. Auletta et al.: "Flexible tape conductor interconnection for chips", pages 1214-1215	

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
12th January 1988	19 FEB 1988
International Searching Authority	Signature of Authorized Officer
EUROPEAN PATENT OFFICE	P.C.G. VAN DER PUTTEN

Form PCT/ISA/210 (second sheet) (January 1985)

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. US 8702473 SA 19089

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 04/02/88
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		WO-A- 8202603	05-08-82
		US-A- 4467400	21-08-84
		US-A- 4479088	23-10-84
		US-A- 4486705	04-12-84
		EP-A- 0175085	26-03-86
US-A- 4426773	24-01-84	JP-A- 57194368	29-11-82